Features

• 240pin, Registered Dual In-line Memory Module (UDIMM)
• Error Check Correction (ECC) Support
• Fast data transfer rates: PC2-4200, PC3-5300, PC3-6400
• Single or Dual rank
• 512MB (64Meg x 72), 1GB(128 Meg x 72), 2GB (256 Meg x 72), 4GB(512Mx72)
• JEDEC standard 1.8V I/O (SSTL_18-compatible)
• V_{DD} = V_{DDQ} = 1.8V ±0.1V
• V_{DDSPD} = 3.0V to 3.6V
• Differential clock inputs, Differential data strobe (DQS, DQS#) option
• 4*n*-bit prefetch architecture
• Multiple internal device banks for concurrent operation
• Programmable CAS latency (CL)
• Posted CAS additive latency (AL)
• WRITE latency = READ latency - 1 tCK
• Programmable burst lengths (BL): 4 or 8
• Adjustable data-output drive strength
• 64ms, 8,192-cycle refresh
• On-die termination (ODT)• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP512MBRRE533O01	512M (64Mx72) 64Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP512MBRRE667O01		PC2-5300	DDR2-667	5-5-5
SP001GBRRE533O01	1GB (128Mx72) 64Mx8 2Ranks	PC2-4200	DDR2-533	4-4-4
SP001GBRRE667O01		PC2-5300	DDR2-667	5-5-5
SP001GBRRE533S01	1GB (128Mx72) 128Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP001GBRRE667S01		PC2-5300	DDR2-667	5-5-5
SP001GBRRE800S01		PC2-6400	DDR2-800	5-5-5
SP002GBRRE533S01	2GB (256Mx72) 128Mx8 2Ranks	PC2-4200	DDR2-533	4-4-4
SP002GBRRE667S01		PC2-5300	DDR2-667	5-5-5
SP002GBRRE800S01		PC2-6400	DDR2-800	5-5-5
SP512MBRRE533P01	512MB (64Mx72) 64Mx4 1Rank	PC2-4200	DDR2-533	4-4-4
SP001GBRRE533R01	1GB (128Mx72) 128Mx4 1Rank	PC2-4200	DDR2-533	4-4-4
SP001GBRRE667R01		PC2-5300	DDR2-667	5-5-5
SP002GBRRE667U01	2GB (256Mx72) 256Mx4 1Rank	PC2-5300	DDR2-667	5-5-5

Note:

1. This document supports all RRE Series DDR2 240Pin UDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP512MBRRE533O01-XX

Pin Assignments

240-Pin DDR2 RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	31	DQ19	61	A4	91	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DDQ}	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	V_{DD}	94	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{SS}	95	DQ42
6	DQS0#	36	DQS3#	66	V_{SS}	96	DQ43
7	DQS0	37	DQS3	67	V_{DD}	97	V_{SS}
8	V_{SS}	38	V_{SS}	68	Par_In	98	DQ48
9	DQ2	39	DQ26	69	V_{DD}	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	SA2
12	DQ8	42	CB0	72	V_{DDQ}	102	NC
13	DQ9	43	CB1	73	WE#	103	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	DQS6#
15	DQS1#	45	DQS8#	75	V_{DDQ}	105	DQS6
16	DQS1	46	DQS8	76	S1#	106	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	DQ50
18	RESET#	48	CB2	78	V_{DDQ}	108	DQ51
19	NC	49	CB3	79	V_{SS}	109	V_{SS}
20	V_{SS}	50	V_{SS}	80	DQ32	110	DQ56
21	DQ10	51	V_{DDQ}	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	V_{SS}	112	V_{SS}
23	V_{SS}	53	V_{DD}	83	DQS4#	113	DQS7#
24	DQ16	541	BA2	84	DQS4	114	DQS7
25	DQ17	55	Err_Out#	85	V_{SS}	115	V_{SS}
26	V_{SS}	56	V_{DDQ}	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	V_{SS}	118	V_{SS}
29	VSS	59	V_{DD}	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

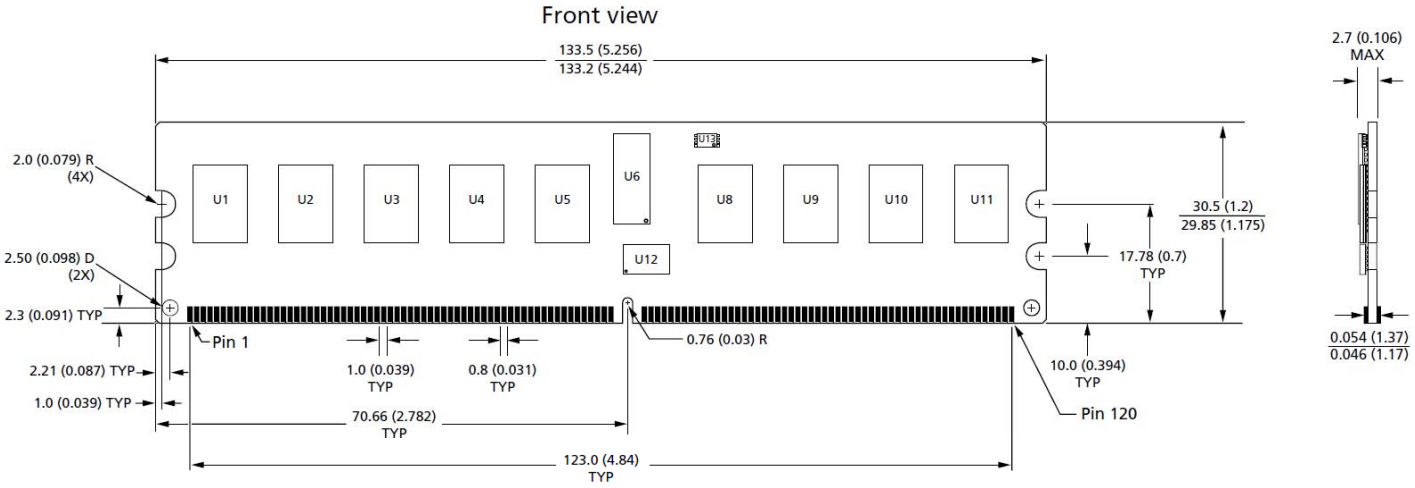
240-Pin DDR2 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	V_{SS}	151	V_{SS}	181	V_{DDQ}	211	DM5/ DQS14
122	DQ4	152	DQ28	182	A3	212	NC/ DQS14#
123	DQ5	153	DQ29	183	A1	213	V_{SS}
124	V_{SS}	154	V_{SS}	184	V_{DD}	214	DQ46
125	DM0/ DQS9	155	DM3/ DQS12	185	CK0	215	DQ47
126	NC/ DQS9#	156	NC/ DQS12#	186	CK0#	216	V_{SS}
127	V_{SS}	157	V_{SS}	187	V_{DD}	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	V_{DD}	219	V_{SS}
130	V_{SS}	160	V_{SS}	190	BA1	220	NC
131	DQ12	161	CB4	191	V_{DDQ}	221	NC
132	DQ13	162	CB5	192	RAS#	222	V_{SS}
133	V_{SS}	163	V_{SS}	193	S0#	223	DM6/ DQS15
134	DM1/ DQS10	164	DM8/ DQS17	194	V_{DDQ}	224	NC/ DQS15#
135	NC/ DQS10#	165	NC/ DQS17#	195	ODT0	225	V_{SS}
136	V_{SS}	166	V_{SS}	196	A13	226	DQ54
137	NC	167	CB6	197	V_{DD}	227	DQ55
138	NC	168	CB7	198	V_{SS}	228	V_{SS}
139	V_{SS}	169	V_{SS}	199	DQ36	229	DQ60
140	DQ14	170	V_{DDQ}	200	DQ37	230	DQ61
141	DQ15	171	CKE1	201	V_{SS}	231	V_{SS}
142	V_{SS}	172	V_{DD}	202	DM4/ DQS13	232	DM7/ DQS16
143	DQ20	173	A15	203	NC/ DQS13#	233	NC/ DQS16#
144	DQ21	174	A14	204	V_{SS}	234	V_{SS}
145	V_{SS}	175	V_{DDQ}	205	DQ38	235	DQ62
146	DM2/ DQS11	176	A12	206	DQ39	236	DQ63
147	NC/ DQS11#	177	A9	207	V_{SS}	237	V_{SS}
148	V_{SS}	178	V_{DD}	208	DQ44	238	V_{DDSPD}
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	V_{SS}	240	SA1

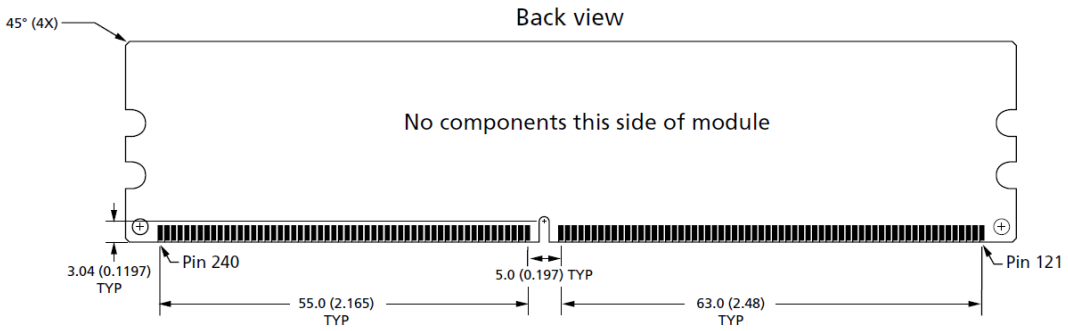
Pin Description

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CKx, CKx#,	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
DMx	I/O	**Data input mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
Err_Out#	Output	**Parity error output:** Parity error found on the command and address bus.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
Sx#, Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** Used to configure the SPD EEPROM address range on the I^2C bus.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage. (VDD/2)
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Simplified Mechanical Drawing(x8 1Rank)

x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs



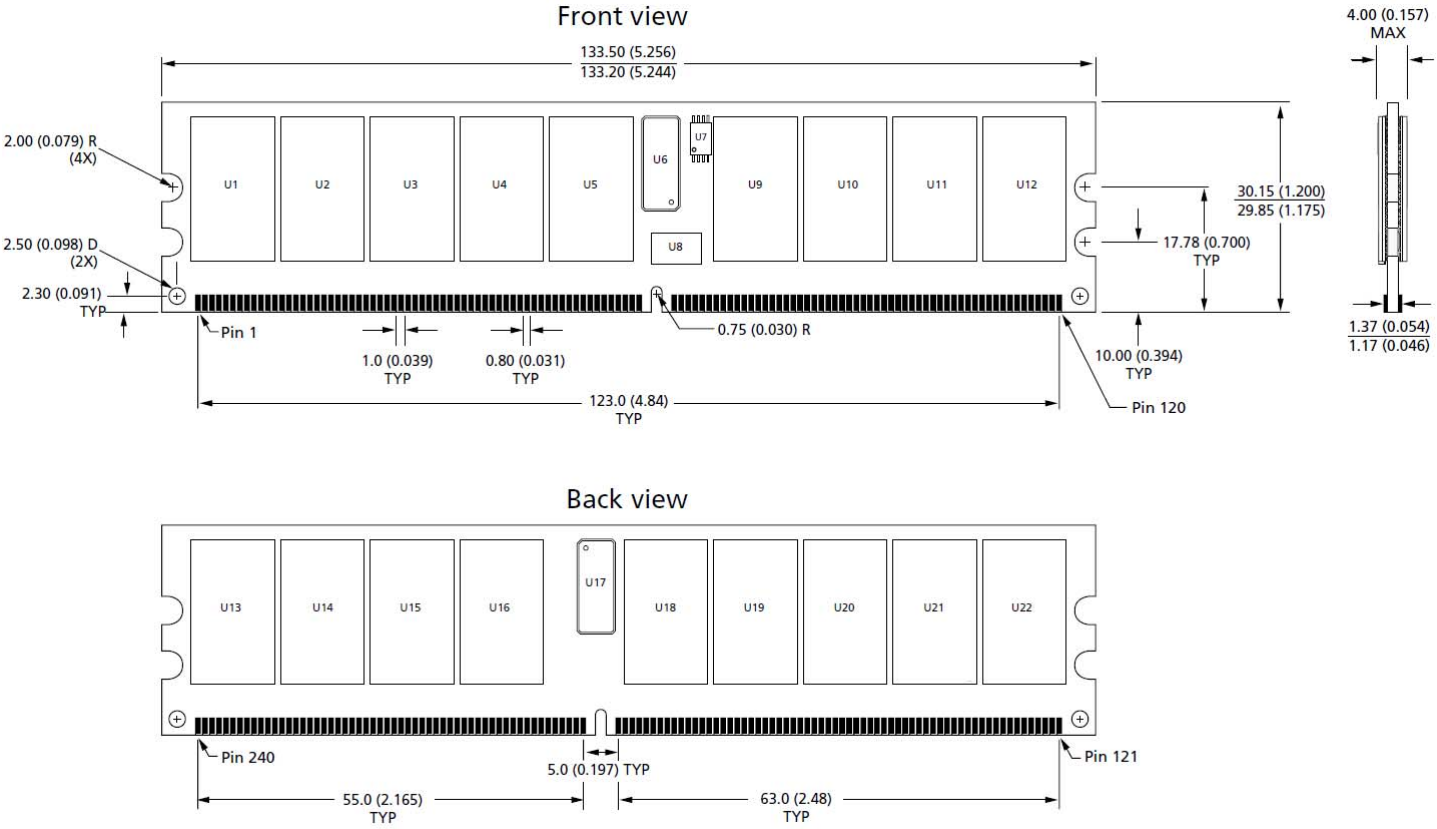


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks / x4 1Rank)

x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs

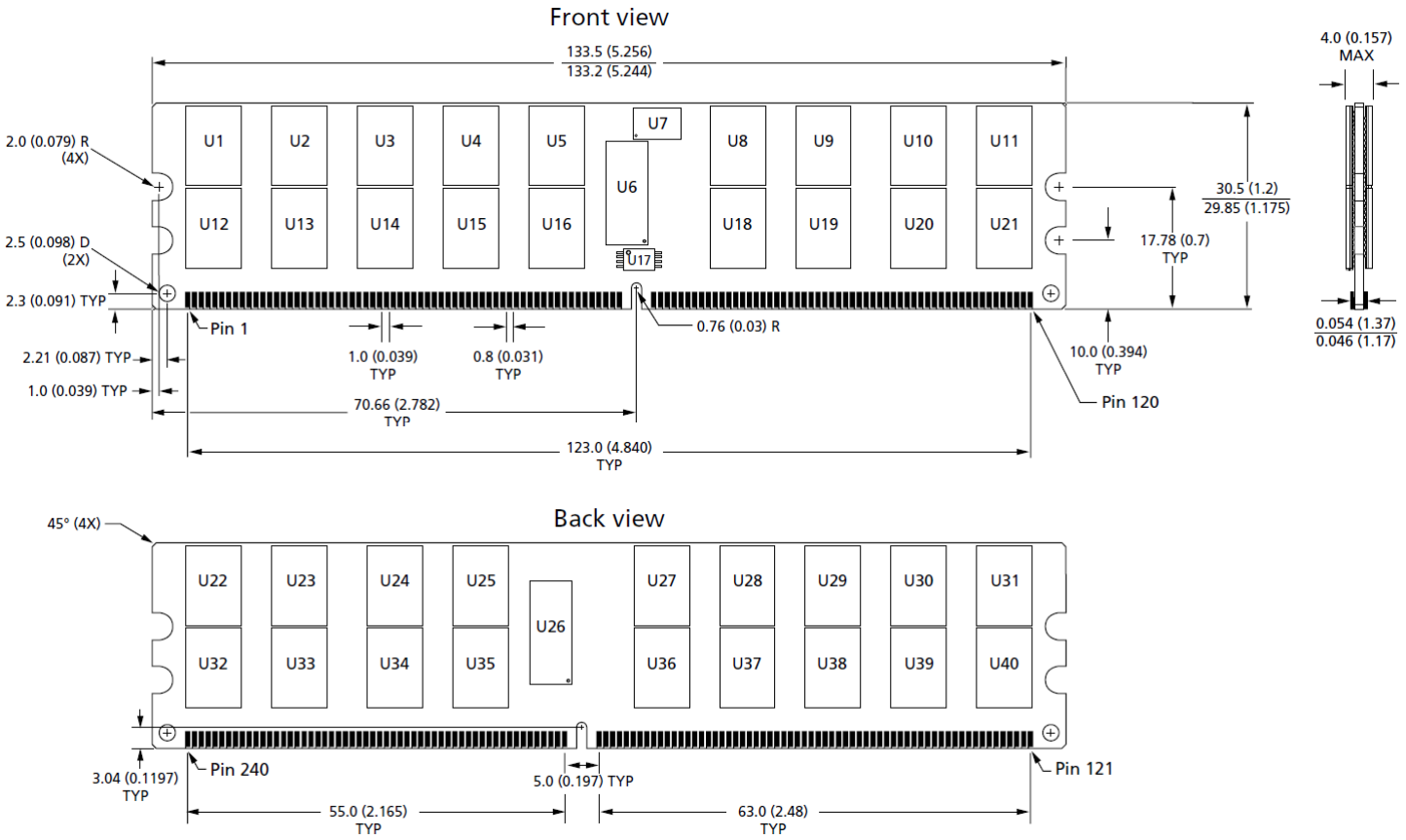


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x4 2Ranks)

x72 DIMM, populated as two physical rank of x4 DDR2 SDRAMs



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.